WHAT IS CLAIMED IS:

1. A method of making a semiconductor device, comprising the steps of:

fabricating a structure that has laterally spaced first and second sections with respective upwardly facing first and second surface portions thereon, and that has a third section projecting upwardly beyond each of said first and second surface portions from a location therebetween;

forming on said structure an insulating layer which has portions disposed over said first and second surface portions, said third section extending into said insulating layer;

effecting a patterned etching of an upper side of said insulating layer using an etch pattern, said etch pattern including an etch region which extends from a location disposed over said first surface portion to a location disposed over said second surface portion, wherein etching in said etch region creates first and second recess portions which respectively extend downwardly through said insulating layer toward said first and second surface portions on opposite sides of said third section;

depositing a conductive material into said first and second recess portions; and

planarizing an upper side of said device at least to a level corresponding to an upper end portion of said third section.

2. A method according to Claim 1, wherein at the start of said step of effecting a patterned etch, an upper surface of said insulating layer is higher than an upper end of said third section.

3. A method according to Claim 1 including, prior to said step of effecting a patterned etch, the step of planarizing said insulating layer to a level corresponding substantially to an upper end of said third section.

4. A method according to Claim 1, wherein said depositing step includes the steps of depositing a first layer of said conductive material, planarizing said first layer by etching said first layer, and thereafter depositing a second layer of said conductive material.

5. A method according to Claim 1, wherein said planarizing step leaves respective portions of said conductive material in each of said first and second recess portions, said portions of said conductive material each serving as a local interconnect through said insulating layer with respect to a respective one of said first and second sections.

6. A method according to Claim 1, wherein said fabricating step includes the step of forming spaced source and drain regions in a semiconductor substrate, said source and drain regions being said first and second sections, and forming on said substrate between said source and drain regions a gate section which includes a gate dielectric layer, a gate electrode over said gate dielectric layer, an insulator layer over said gate electrode, and insulator sidewalls on opposite sides of said gate dielectric layer, said gate electrode and said insulating layer, said gate section being said third section.

7. A method according to Claim 6, including after said step of forming said insulator layer, the step of creating an opening through said insulator layer.

8. A method according to Claim 6, wherein said step of forming said insulator layer on said gate electrode is carried out by forming alternating layers of a nitride material and an oxide material.

9. A method according to Claim 1, wherein said etch pattern has at least one etch-resistant island provided within said etch region and disposed above one of said first and second surface portions.

10. A method of making a semiconductor device, comprising the steps of:

fabricating a structure having laterally spaced first, second and third sections with respective upwardly facing first, second and third surface portions thereon, said second section being disposed between said first and third sections, said structure further having a fourth section projecting upwardly beyond each of said first and second surface portions from a location therebetween, and a fifth section projecting upwardly beyond each of said second and third surface portions from a location therebetween;

forming on said structure an insulating layer which has portions disposed over each of said first, second and third surface portions, said third and fourth sections extending into said insulating layer;

effecting a patterned etching of an upper side of said insulating layer using an etch pattern, said etch pattern including an etch region which extends from a location disposed over said first surface portion through a location disposed over said second surface portion to a location disposed over said third surface portion, wherein etching in said etch region creates a first recess portion which extends downwardly through said insulating layer toward said first surface portion adjacent said fourth section, a second recess portion which extends downwardly through said insulating layer toward said second surface portion adjacent said fourth and fifth sections, and a third recess portion which extends downwardly through said insulating layer toward said third surface portion adjacent said fifth section;

depositing a conductive material into said first, second and third recess portions; and

planarizing an upper side of said device at least to a level corresponding to upper end portions of said fourth and fifth sections.

11. A method according to Claim 10, wherein at the start of said step of effecting a patterned etch, an upper surface of said insulating layer is higher than upper ends of said fourth and fifth sections.

12. A method according to Claim 10 including, prior to said step of effecting a patterned etch, the step of planarizing said insulating layer to a level corresponding substantially to upper ends of said fourth and fifth sections.

13. A method according to Claim 10, wherein said depositing step includes the steps of depositing a first layer of said conductive material, planarizing said first layer by etching said first layer, and thereafter depositing a second layer of said conductive material.

14. A method according to Claim 10, wherein said planarizing step leaves respective portions of said conductive material in each of said first, second and third recess portions, said portions of said conductive material each serving as a local interconnect through said insulating layer with respect to a respective one of said first, second and third sections.

15. A method according to Claim 10, wherein said fabricating step includes the steps of:

forming spaced source and drain regions in a semiconductor substrate, each of said first, second and third sections being a respective one of said source and drain regions;

forming said fourth section by forming on said substrate between said first and second regions a first gate dielectric layer, forming a first gate electrode over said first gate dielectric layer, forming a first insulator layer over said first gate electrode, and forming first insulator sidewalls on opposite sides of said first gate dielectric layer, said first gate electrode and said first insulating layer; and

forming said fifth section by forming on said substrate between said second and third regions a second gate dielectric layer, forming a second gate electrode over said second gate dielectric layer, forming a second insulator layer over said second gate electrode, and forming second insulator sidewalls on opposite sides of said second gate dielectric layer, said second gate electrode and said second insulating layer.

16. A method according to Claim 15, wherein said step of forming each of said first and second insulator layers is carried out by forming alternating layers of a nitride material and an oxide material.

17. A method according to Claim 11, wherein said etch pattern has at least one etch-resistant island provided within said etch region and disposed above one of said first, second and third surface portions.

18. An apparatus comprising a semiconductor device which includes:

laterally spaced first and second sections with respective upwardly facing first and second surface portions thereon;

a third section projecting upwardly beyond each of said first and second surface portions from a location therebetween, said third section having two side surfaces on opposite sides thereof;

an insulating layer which has portions disposed over said first and second surface portions, said third section extending into said insulating layer, and said insulating layer having first and second recess portions which respectively extend downwardly through said insulating layer toward said first and second surface portions on opposite sides of said third section, each said recess portion being immediately adjacent a respective said side surface of said third section;

a first portion of conductive material disposed in said first recess portion; and

a second portion of conductive material disposed in said second recess portion.

19. An apparatus according to Claim 18, including a semiconductor substrate having spaced source and drain regions which serve as said first and second sections, and including between said source and drain regions a gate section which includes a gate dielectric layer, a gate electrode over said gate dielectric layer, an insulator layer over said gate electrode, and insulator sidewalls on opposite sides of said gate dielectric layer, said gate electrode, and said insulator layer, wherein said gate section is said third section.

20. An apparatus according to Claim 19, wherein said first and second portions of conductive material have respective upwardly facing third and fourth surface portions thereon, said third and fourth surface portions being substantially coplanar with a top surface of said insulator layer.

21. An apparatus according to Claim 19, wherein said insulator layer includes alternating layers of a nitride and an oxide.

22. An apparatus according to Claim 18, wherein said side surfaces are spaced by a distance which corresponds to a minimum gate length in said semiconductor device.